Change log

Name of the submission: DryGASCON

Changes between round 1 submission package and round 2 submission package:

- C99 code:
    - "le32" implementation modified to avoid problems related to "strict aliasing" rules.
    - supercop’s optional files added
- python3 code: aead.py corrected to handle correctly last argument (verbosity level).
- verilog code: simulation script for Xilinx XSIM (Vivado’s free simulator).
- hx8k FPGA full source code and quick start guide